

REMARKS

Proposed drawing corrections Figs. 1, 2, 4, and 7 are enclosed. In regard to Fig. 6, there is no element 85e and the specification has been amended accordingly. The specification is also amended to overcome the Examiner's objections and to correct some errors noted by Applicants.

Claims 1-24 remain in this application. Claim 9 has been amended to correct the typographical error noted by the Examiner. Claims 1-3, 6, 9 and 17-19 have been rejected. The Examiner has indicated that claims 4, 5, 7, 8, 10-16 and 20-24 would be allowable if in independent form. Applicants appreciate this indication of allowability, but have not amended these claims, since, for the reasons set out in detail below, it is believed that all claims are in condition for allowance.

The Examiner asserts that claims 1 and 2 are anticipated by Therssen. Applicants respectfully traverse this rejection. The method claimed in claimed 1 is a method for recovering phase information. In contrast, Therssen is directed to converting a sampling frequency used in digital audio. More importantly, the specifically claimed elements in the body of the claims are not found in the reference. The first limitation of "over-sampling data transmitted at a first frequency using a clock at a second frequency to obtain groups of n samples" is not met. Sampling does take place at a second frequency. The samples would be the d_N of Figs. 3 and 4 output by decimation filter 42. However, there is no teaching of obtaining groups of n samples. The N is the N times higher sampling frequency. The process is continuous and does not deal with obtaining and operating on groups of samples.

Also consider what happens to the samples in the reference next. The frequency is reduced by a factor M resulting in missing pulses. The FIFO is used to get equal spacing of the pulses, which are read in at one frequency and read out at another. There is no "storing a plurality of m of said groups of n samples," as required by claim 1. In the variation shown in Fig. 8, this also does not occur. In that embodiment samples are stored at the frequency of the incoming signal and read out at the final output frequency

multiplied by M/N . There is no teaching of storing n groups of n samples. Again, this is a continuous process with data continuously being clocked in and out of the FIFO.

This leads to the last claim limitation in claim 1: "outputting said plurality of m of said groups of n samples simultaneously at a clock frequency which is said second frequency divided by m ." First, Applicants note that in Fig. 3 of the reference, data is read into the FIFO at the frequency N/M . In Fig. 8, data is read out of the FIFO at the rate of M/N . Secondly in the claim n is a number of samples. In the reference it is a frequency. Finally, according to the claim m groups of n samples must be read out simultaneously. It seems quite clear that this does not happen in the reference.

Thus, claim 1 and claim 2 dependent thereon (the limitations of which are also not present as should be evident from the discussion above) are not anticipated and should be allowed. Similarly, claims 3 and 6, which depend on claim 2 are allowable. Nothing in the secondary reference makes up for the deficiencies in Therssen.

Claim 9 has the essential limitations discussed above. The Examiner has applied Therssen in the same way as to claim 1. For the same reasons set out above, these limitations are not found in Therssen. Nor does Jeong make up for the missing teaching. Thus, claim 9 is also allowable. In like fashion claim 17 and dependent claims 18-19 are allowable. Once again neither reference teaches the m groups of n samples claimed in these claims.

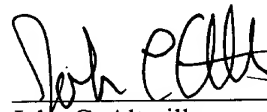
In view of the above, Applicants submit that, as amended, the remaining claims clearly distinguish over the art and are in condition for allowance.

The Examiner is invited to call the undersigned at (202) 220-4200 to discuss any information concerning this application.

The Office is hereby authorized to charge any additional fees under 37 C.F.R.
§ 1.16 or § 1.17 or credit any overpayment to Deposit Account No. 11-0600.

Respectfully submitted,

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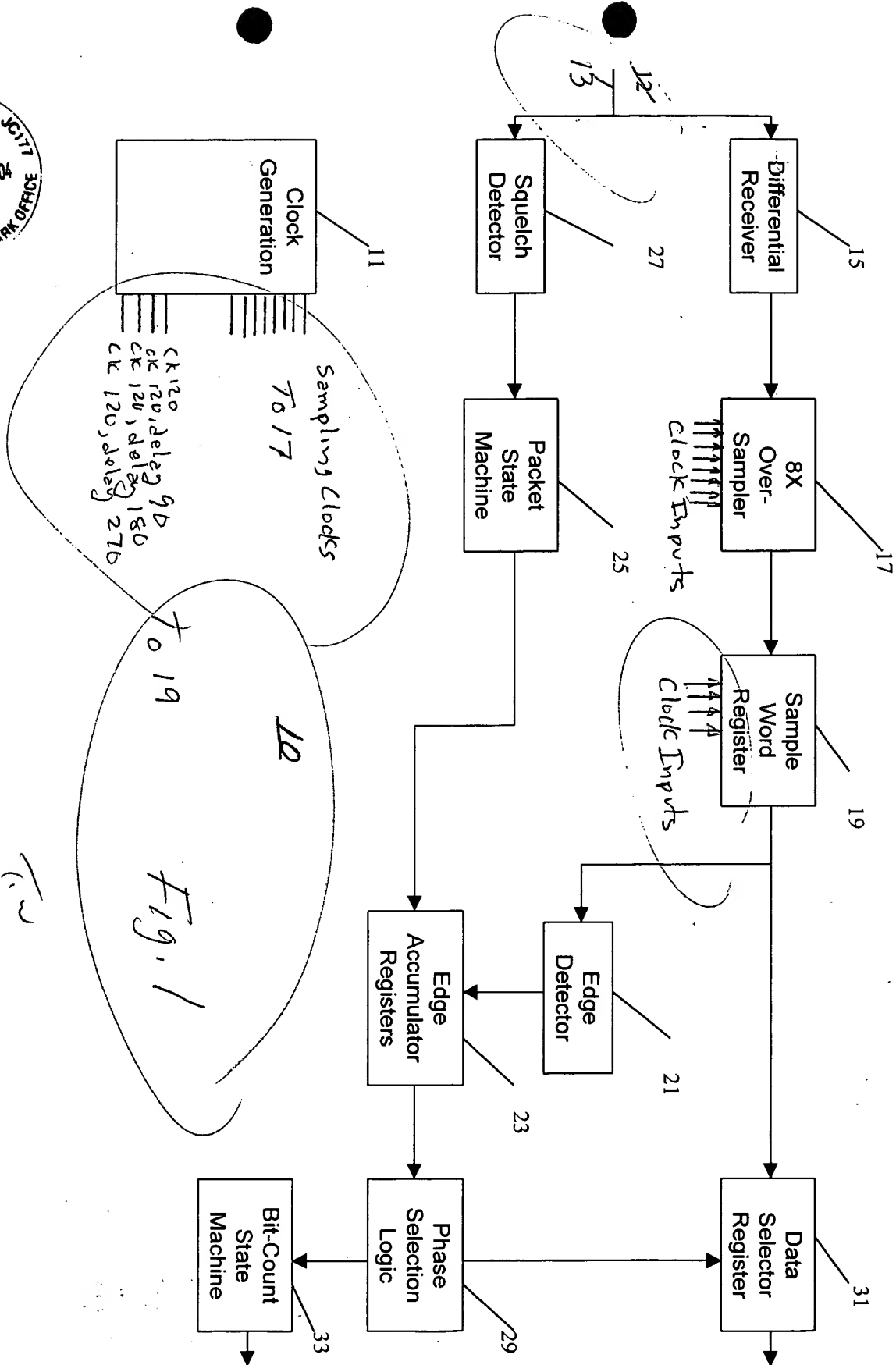
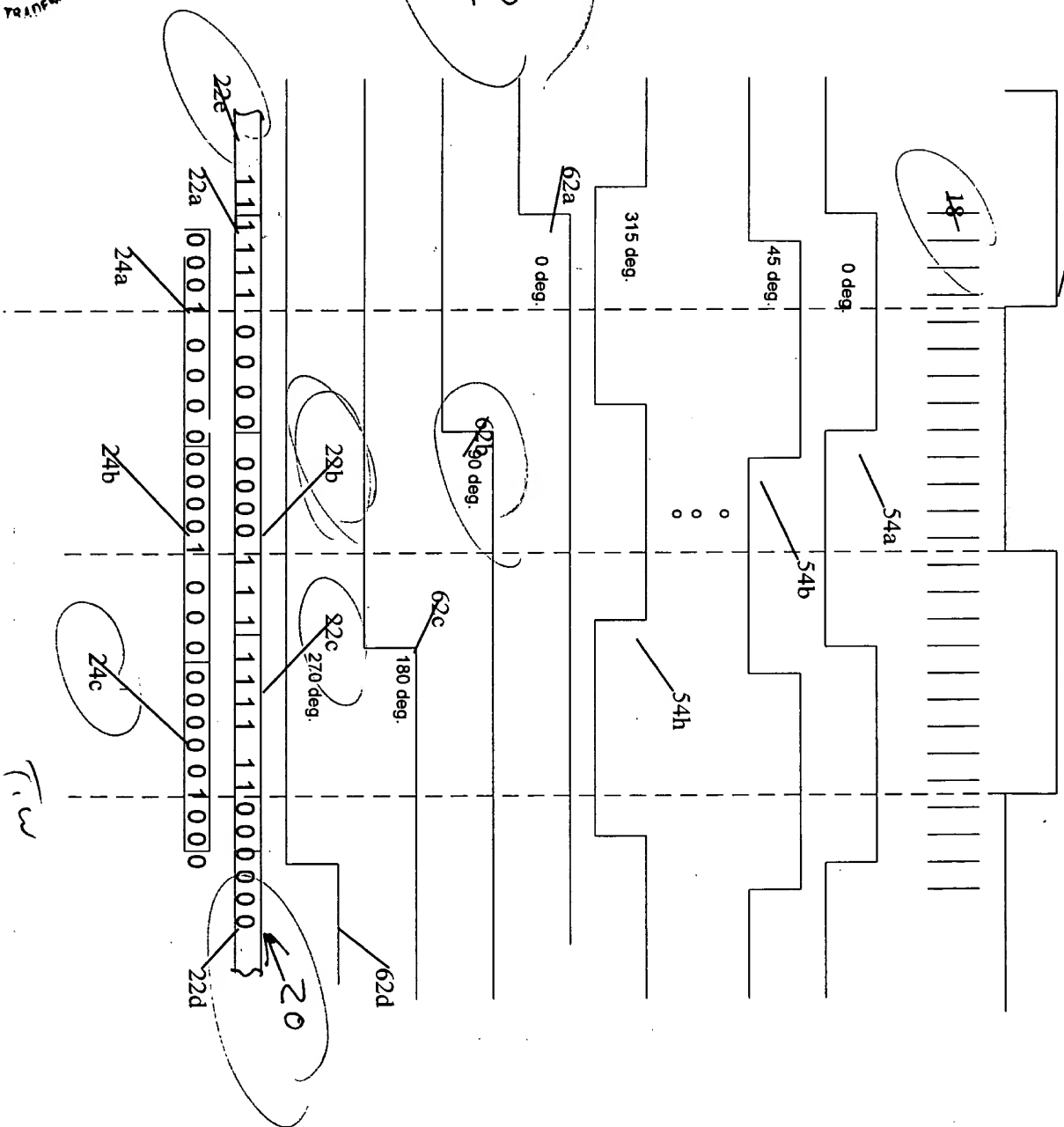
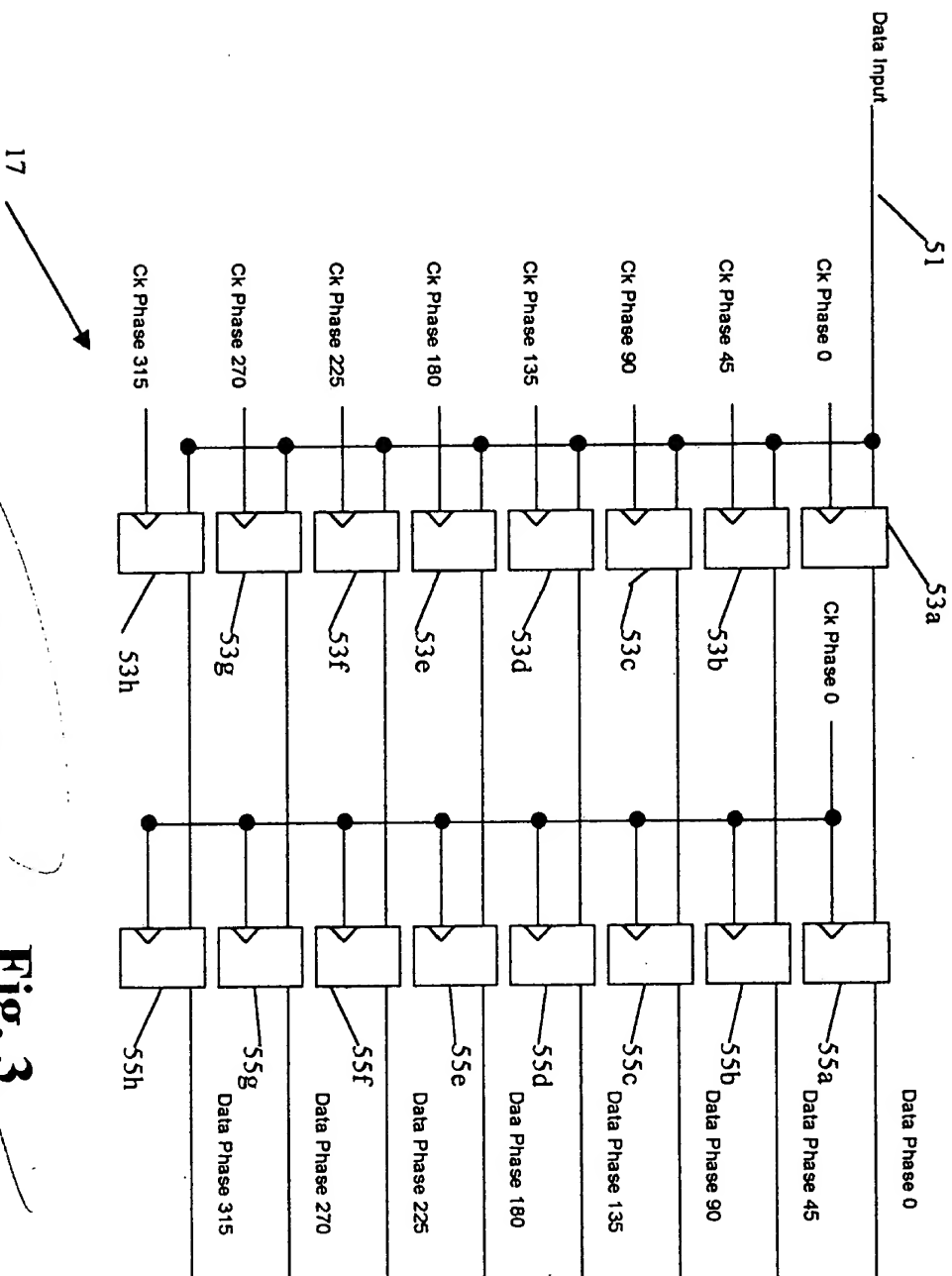


Fig. 2





8X Over-Sampler

Fig. 3

Tim

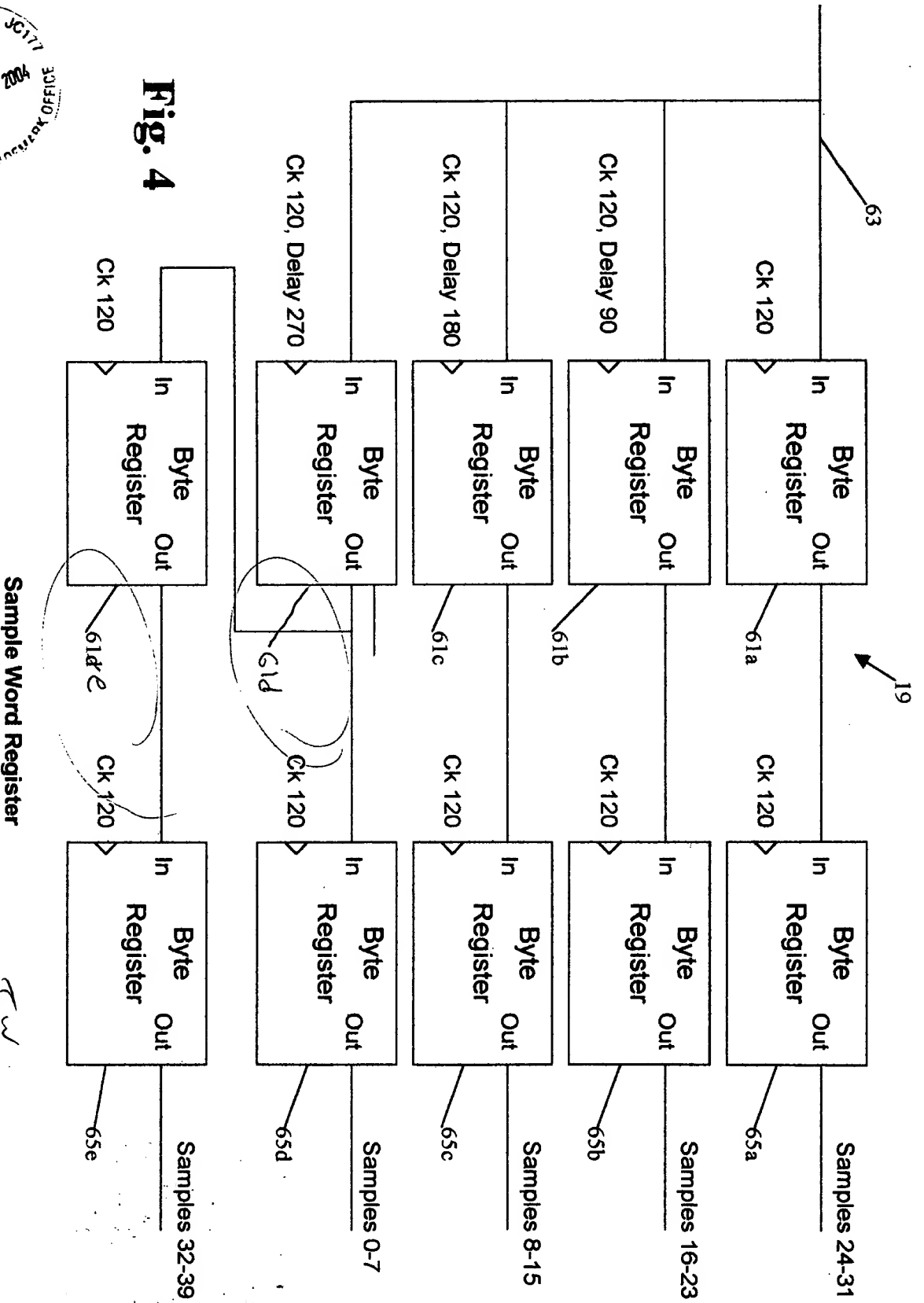


Fig. 4



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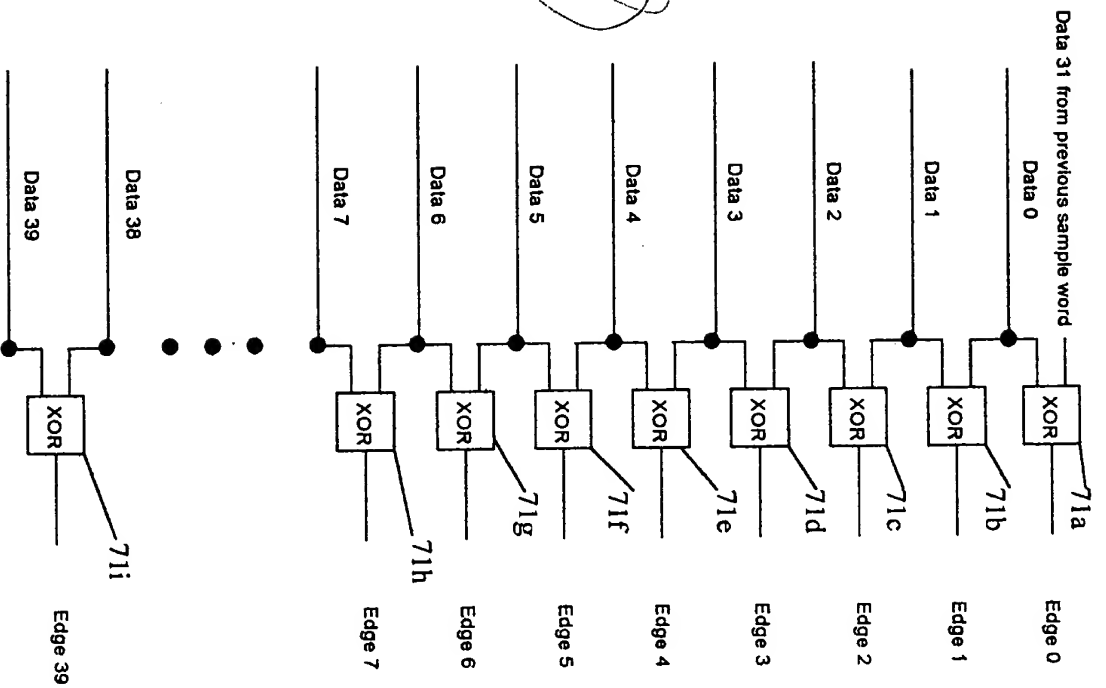
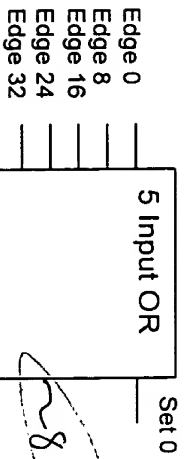


Fig. 5

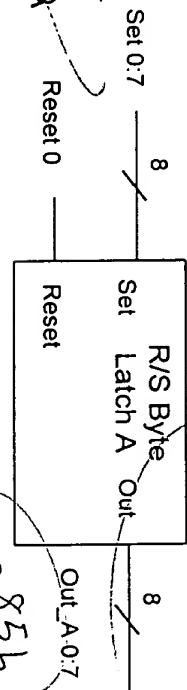
Edge Detector

71i

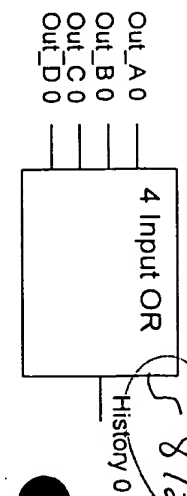
8 - 5 Input OR Gates



4 - Edge Accumulator Registers

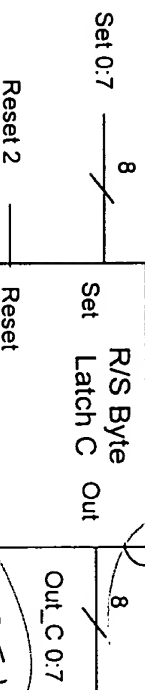


8 - 4 Input OR Gates



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Reset 2

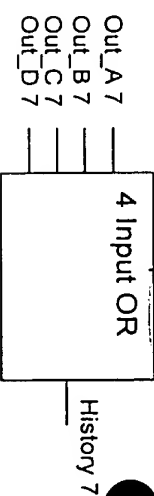
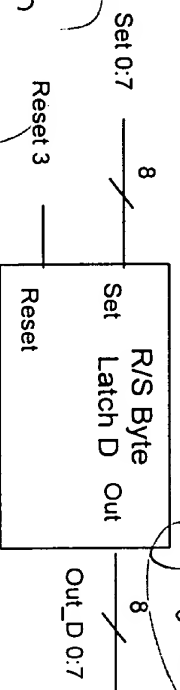
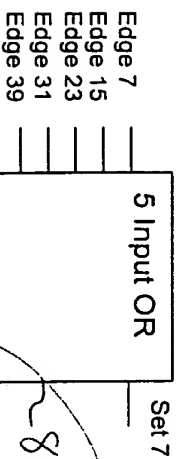
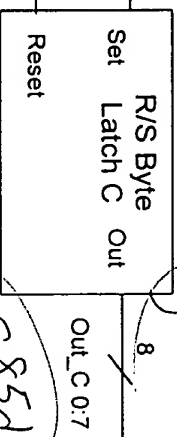


Fig. 6

Edge Accumulator Register

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History 0:7

Each history bit OR'd with following bit (latest OR'd with earliest)

91 8

93 Highest Byte

Each bit from above OR'd with bit on either side (first and last wrap around)

95

97 2nd Highest Byte

Each bit from above OR'd with bit on either side (first and last wrap around)

99

101 3rd Highest Byte

Logic which determines the highest level byte which has 2 or less zeroes, and outputs the following:

- 1) phase of the sole remaining 0 if only one
- 2) phase of the latest 0 if adjacent pair remains
- 3) error indication if 2 non-adjacent 0's remain

103

Limit Max Phase Change to +/- 1 Sample Phase

105

Selected Sample Phase

107

Phase Selector

Fig. 7



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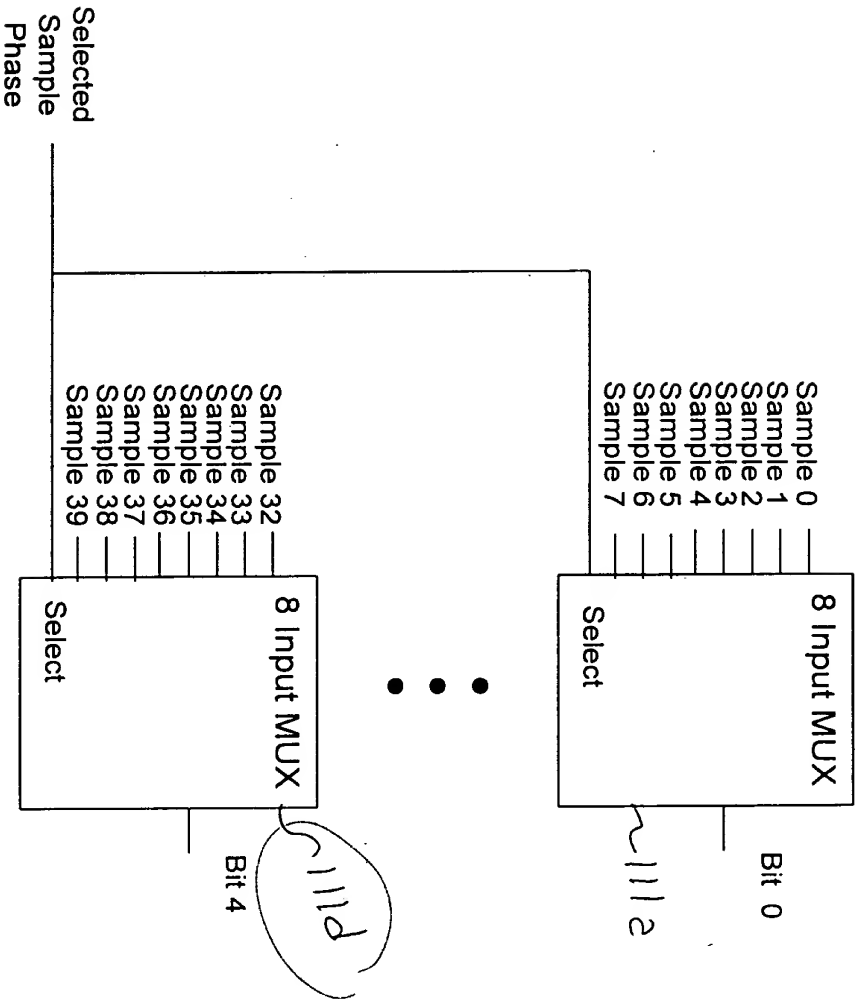


Fig. 8

Data Selector Register

π. v

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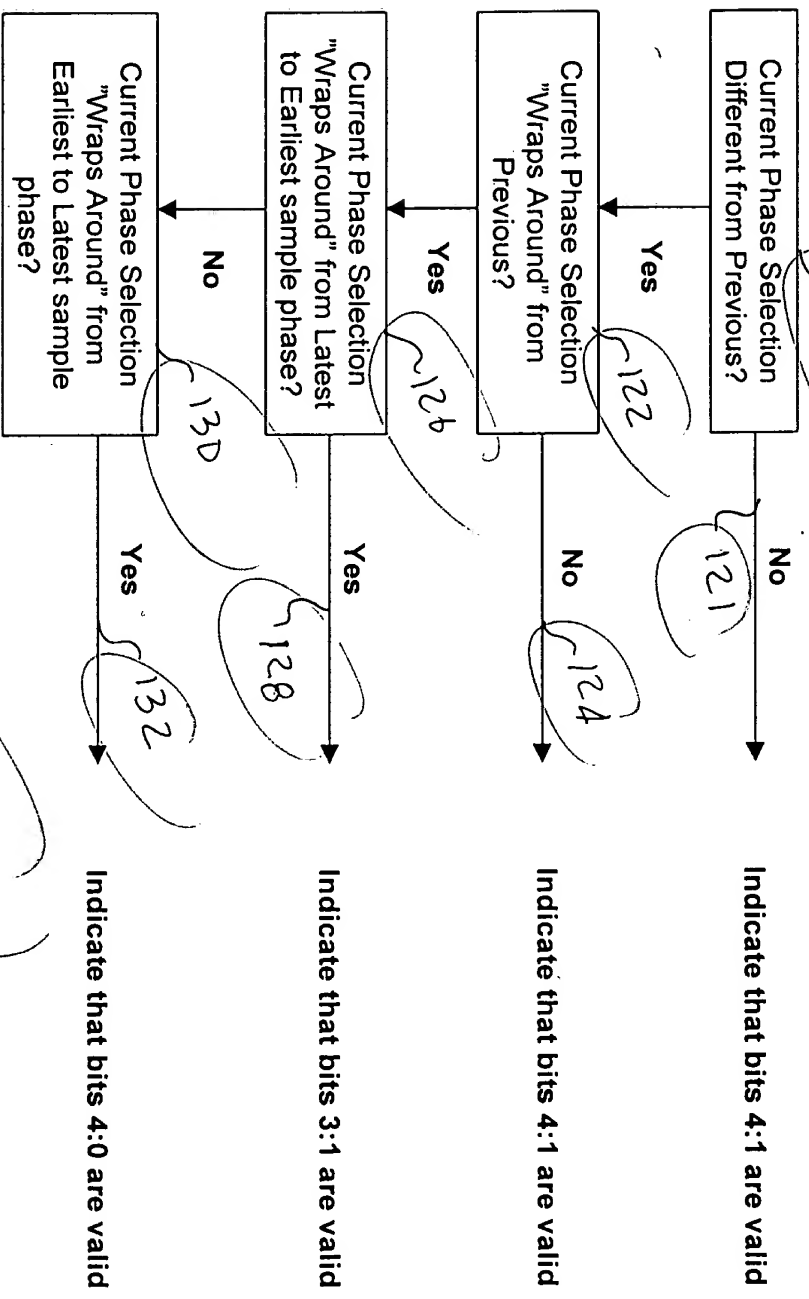


Fig. 9

Bit Count State Machine